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| EXAMINER | |
|---|---|
| NATALINI, JEFF WILLIAM | |
| **ART UNIT** | **PAPER NUMBER** |
| 2858 | |

DATE MAILED: 04/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/810,645 | KER ET AL. | |
| | Examiner | Art Unit | |
| | Jeff Natalini | 2858 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *4/10/06*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 5, 15, and 21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. These claims specifically claim that the pulse generator includes a biasing source to generate the second ESD scale pulse. As was discussed in the arguments filed 4/3/06 and the phone interview 4/10/06, a bias source is known in the art to generate a constant DC voltage or current to set a semiconductor device to a desired operation. A source that generates an ESD scale pulse will not be considered a "bias source". The definition of a bias source in electrical engineering (from wikipedia.com) is "bias simply refers to a fixed DC voltage applied to the same point in a circuit as an AC signal, to select the desired operating response of a semiconductor (forward or reverse bias). For example, a bias voltage is applied to a transistor in an electronic amplifier to allow the transistor to operate in a particular region of its transconductance curve". A pulse as discussed in the phone interview is a current or voltage which changes abruptly from one value to another and back to the orginal value in a finite length of

time. This would not be produced by a "bias" source as known in the art (the specification and drawings also contain this informality and are therefore objected to).

***Drawings***

The drawings are objected to because the bias circuit is generating an ESD-scale pulse (see above 35 U.S.C. 112, first paragraph rejection), this should be changed to simply be a pulse generator generating a pulse (specifically figures 5 and 6). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Specification*

The specification is objected to because the specification states in multiple places that the bias circuit is generating an ESD-scale pulse (see above 35 U.S.C. 112, first paragraph rejection).

### *Claim Objections*

3. Claims 1 and 12 are objected to because of the following informalities:

In regard to claim 1, it must be stated how the data collector is associated with the rest of the circuitry in the invention, for example.. "a data collector, connected to the semiconductor device, to collect data on the ESD characteristics of the semiconductor device".

In regard to claim 12, it must be stated how the detector is associated with the rest of the circuitry in the invention (see above objection to claim 1).

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 31-34 is rejected under 35 U.S.C. 102(b) as being anticipated by Itoh (5561373).

In regard to claim 31, Itoh discloses a method of electrostatic discharge (ESD) testing (abstract), comprising: providing a multi-terminal device (fig 1a); generating at least two ESD-scale pulses (col 2 line 64-col 3 line 10, pulse is seen in fig 1c); providing a first ESD-scale pulse of the at least one ESD-scale pulses to a first and a second terminals of the multi-terminal device (col 4 line 52-64, fig 1a); providing a second ESD-scale pulse of the at least one ESD-scale pulses to at least a third terminal of the multi-terminal device (col 4 line 52-64 and col 2 line 64-col 3 line 10 and fig 1a, there will be an ESD pulse applied to each of the terminals at one time and then soon after (in the next production process) there will be a second ESD pulse applied to each of the terminals); collecting ESD characteristics of the multi-terminal device under the first and second ESD-scale pulses (col 2 line 64-col 3 line 10); and detecting if a leakage current flows in the multi-terminal semiconductor device (col 4 line 54-col 5 line 8).

In regard to claim 32, Itoh discloses wherein a bipolar junction transistor is the device under test (col 4 line 62-64).

In regard to claim 33, Itoh discloses wherein the step of providing the second ESD scale pulse to at least one third terminal before providing the first ESD scale pulse to the first and second terminals (col 4 line 52-64, col 2 line 64-col 3 line 10, fig 1a; a pulse is applied to all the terminals at one time (could broadly be second pluse) and then at a later time another pulse (could broadly be first pulse) is applied to all the terminals.

In regard to claim 34, Itoh discloses a step of detecting whether a leakage current flows in the multi-terminal device before providing the first and second ESD-

scale pulses (col 4 line 64-col 3 line 10; states after stresses are applied the leakage current may be increased, in order to make that determination there must have been a detection of the leakage current before the ESD pulse was applied).

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-5, 9, 10, 12-15, 17-22, 26-29, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh (5561373) in view of Chen et al. (Investigation of the Gate-driven ... IEEE article).

In regard to claims 1, 3, 4, 10, 12-14, 18-20, 28, 29, and 35, Itoh discloses (all that is disclosed in the rejection above for claim 34-for the rejection of claim 35) a system/method for measuring electrostatic discharge characteristics of a semiconductor device (abstract) comprising: a first point of the semiconductor device receiving a first ESD-scale pulse (col 4 line 52-64, fig 1a); a second point of the semiconductor device receiving the first ESD-scale pulse (col 4 line 52-64, fig 1a); at least a third point of the semiconductor device receiving a second ESD-scale pulse (col 4 line 52-64 and col 2 line 64-col 3 line 10 and fig 1a, there will be an ESD pulse applied to each of the terminals at one time and then soon after (in the next production process); and a data collector to collect data on the ESD characteristics of the semiconductor device (col 4

line 65-col 5 line 28); a detector to detect a leakage current of the semiconductor device where the ESD characteristics of the multi-terminal device are determined when the detector detects a leakage current in the device (col 4 line 54-col 5 line 8).

Itoh lacks wherein the ESD pulses are generated by at least one pulse generator, specifically wherein this pulse generator is a TLP.

Chen et al. discloses testing ESD robustness of semiconductor devices using a TLP generator (abstract, pg 193 last paragraph continued to pg 194).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Itoh to incorporate using a TLP generator for testing static properties as taught by Chen et al. in order to be able to generate a pulse on demand for analyzing the breakdown characteristics and turn on resistance of the semiconductor device (pg 193 last paragraph continued to pg 194, fig 8 on pg 194).

In regard to claims 2, 17, and 22, Itoh discloses wherein a bipolar junction transistor is the device under test (col 4 line 62-64).

In regard to claim 9 and 27, Itoh discloses wherein providing the first ESD scale signal to a emitter and collector of the BJT (col 4 line 52-64), and providing the second ESD scale signal to a base of the BJT (col 4 line 52-64).

In regard to claim 26, Itoh as modified by Chen et al. lacks wherein a FOD is specifically the semiconductor device to be tested. It would have been obvious to one with ordinary skill in the art at the time the invention was made to use engineering intuition knowing that a FOD is similar to a BJT to test a FOD similarly to the BJT test in order to properly test semiconductor devices for electrostatic discharge.

8. Claims 6 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh (5561373) in view of Chen et al. as disclosed in claim 2 above, and further in view of Mishra et al. (5872031).

Itoh discloses wherein a MIS (metal insulator semiconductor) includes a source and a drain to receive the first ESD scale pulse (fig 1-P2 and P3, col 4 line 52-54) and at least one of a gate and a substrate to receive the second ESD scale pulse (fig 1-P1 and P4). It is understood in the art the MIS and MOS have equivalent functionality in the art and could be interchangeable (seen in Mishra et al. col 5 line 15-20).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Itoh as modified to use a MOS instead of a MIS in testing of the semiconductor device as taught by Mishra et al. because they have similar logic characteristics (col 5 line 15-20).

9. Claims 7, 8, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh (5561373) in view of Chen et al. as disclosed in claim 2 above, and further in view of Ker et al. (US 5576557).

Itoh as modified by Chen et al. lacks wherein an SCR and LVTSCR includes an anode and a cathode to receive the first ESD pulses, and a substrate to receive a second ESD pulse.

Ker et al. teaches SCR and LVTSCR includes an anode and a cathode to receive an ESD pulse, and a substrate to receive a second ESD pulse.

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Itoh as modified to include testing a SCR and LVTSCR with an anode and cathode to receive an ESD pulse, and a substrate to receive a second ESD pulse as disclosed by Ker et al. in order to be able to provide proper protection to CMOS ICs (col 1 line 11-15).

10. Claims 11, 16, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh (5561373) in view of Chen et al. as disclosed in claim 1 above, and further in view of Consiglio (US 5519327).

Itoh as modified by Chen et al. lacks wherein there is a switching device coupled to the pulse generator(s) and the detector to switch a connection between the pulse generator(s) and the detector.

Consiglio teaches having a switch coupled between a pulse generator and the detector to detect the leakage current so to switch the connection between the pulse generator and the detector (fig 3, chart; abstract).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Itoh as modified to include a switch coupled between a pulse generator and the detector to detect the leakage current as taught by Consiglio in order to determine the leakage current after each pulse is applied to the DUT (abstract).

***Response to Arguments***

11. Applicant's arguments (arguments filed 4/3/06 and the phone interview 4/10/06) with respect to claims 1-35 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Natalini whose telephone number is 571-272-2266. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diane Lee can be reached on 571-272-2399. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeff Natalini

ANJAN DEB
PRIMARY EXAMINER